Thermoelectric Micro Devices: Current State, Recent Developments and Future Aspects for Technological Progress and Applications

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Abstract

Due to their unique expected properties thermoelectric microdevices, thermogenerators as well as Peltier coolers, are of high demand for different applications namely for telecommunication purposes. Thus worldwide efforts are undertaken to expand the technology for thermoelectric devices into the field of typical microsystem technologies including aspects of advanced low dimensional high ZT materials. Favourite material systems are up to now the bismuthtelluride (V-VI) compounds and the silicon/germanium (IV-IV) alloys. Recent results prove the capability to implement low dimensional material of both material systems into microsystem devices and demonstrate wafer based microelectronic technologies for the fabrication of thermoelectric devices even for the non CMOS bismuthtelluride related compounds. Thus this survey will present the state of the art [1-9] in a summary of recent results together with an more extended description of the MicroPelt® approach as an example for a wafer based fabrication concept close to microelectronics manufacturing. Strengths and weaknesses of the different presented technological concepts will be discussed under some viewpoints.

Introduction

Regardless of the actual intermediate depression of the telecommunation market, this market will be a major driving economic force in the future. Together with the oncoming more powerful PC processors these two examples may illustrate the expected increasing demand of miniaturized coolers with cooling power densities around and above 100W/cm^2. Basics and also details may be found in [10,11,12] and literature cited therein. Even though the progress for MicroElectroMechanicalSystems (MEMS) or nanoscale ThermoElectricConverters (TEC), here peltier and generator devices, was pillared essentially by an academic character for a long period nowadays the tendency changes. This is in evidence looking at the emerging wafer based technologies [4,13,14,15] with their orientation to further consumer markets like Infineon's announced innovations in electronics for textiles, i.e. smart cloths [16]. This overview will start with a new illustration of a qualification plot to support the design for various technologies for micro-TEC. In a short summary the actual wafer-technology approaches will be presented and finally a new wafer approach for thick thin-film TEC devices [15] will be described in more detail.

Qualification Plot for MicroTEC's

Some of the parameters which influence the performance of micro-TECs are described in [10,11,12,14]. These are e.g. the cooling power density as function of temperature difference across the cooler-device [10,14], in particular the dependence on the height of thermocouple [10], or the limitations for close packed thermocouples on a substrate, dependent on the thermal conductivity of different substrates [11,13]. If one considres in detail the problems of a micro-TEC fabrication a lot of more design and technological parameters are important which will also influence the performance of the particular device.

Thus Fraunhofer IPM developed an extended simulation tool resulting in various qualification plots for micro-TEC technologies [17]. The data setup for this simulation comprises all necessary geometrical design parameters for all components of the device and technologically important physical parameters like Seebeck coefficients, thermal- and electrical conductivities of the layers accordingly. Depending on the particular technology, the set of design and physical parameters may be extended or lessened. Based on those sets of parameters, all interesting performance features were calculated. They were summarised and plotted in an n-fold performance (star)-diagramms, fig. 1-3.

We decide to plot an six-fold star, taking from our point

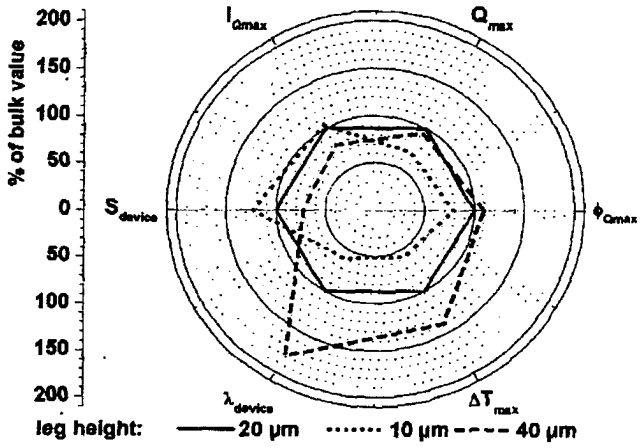

Figure 1. Performance qualification plot for different leg heights.

of view, the most important six performance parameters: the maximum heat flux (Q_{max}) at a given temperature difference across the device (here for example ΔT=10K), the efficiency φ at Q_{max} (φ (Q_{max})), the current I at Q_{max} (I(Q_{max})), the sum

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of the electrical conductivities, S_{device}, the sum of the thermal resistance including hot side thermal resistance, λ_{device}, and ΔT_{max} at zero heat flux.

For each fig. 1-3 an internal 100% standard (named "bulk value" in fig. 1-3) was fixed. For all fig. 1-3 the material data for good bulk material ZT around 1 for room temperature were taken. In case of fig. 1 the contact resistance was set as $R_c=10^{-10}\Omega m^2$, a Si wafer was assumed as substrate and the height of the thermocouple for the 100% value was set to 20μm. Figure 1 shows the qualification plot for various thermocouple heights, for vertically integrated modules. The influence of either thinner or thicker thermocouples, calculated in "%" in relation to the internal standard, is easy to read off.

In the case of the 40 μm thermocouple height the decrease of Q_{max} is caused by an increase in Joule heating due to an increase in electrical resistance which outranges the increase in thermal resistance. The increase in ΔT_{max} is directly correlated to this increase of thermal resistance. In the case of the 10 μm thick device the decrease in Q_{max} is caused by the increasing influence of Joule heating due to the increasing importance of the contact resistance. Similar to the influence on Q_{max} one can explain the results for the other ploted performance parameters.

A corresponding plot may be derived by varied contact resistances here for a leg height of 20 μm. Figure 2 shows the results respectively. It is obvious that R_c values of $10^{-9}\ \Omega m^2$

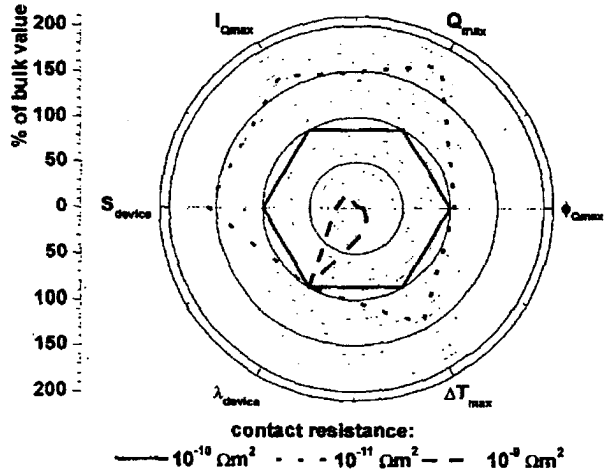

Figure 2. Performance qualification plot for different contact resistances, thermocouple height =20μm

are useless.

To take advantage of the possible cooling power denstity of micro TECs one has to chose suitable substrates. On one hand one has to optimize the heat spreading at the TEC hot side on the other hand technological requirements have to be fulfilled. These are e.g. features like simple, easy and cheap availability, mechanical and thermal stability, compatibility of thermal expansion coefficients etc.. The most common substrate in microelectronics is nowadays silicon, which is available up to 8" and down to thickness of much less than 50μm.

Thus silicon is very attractive as wafer material for this technological approach. To get a better feeling for substrate influence on the above performance parameters, figure 3 demonstrates the corresponding results. Figure 3 shows, that it might be better to built up a technological route on cheap thin silicon wafers than on diamond ones. The increase for ΔT_{max} and for Q_{max} from comparatively thick silicon of 200 μm to a diamond wafer with the same thickness amounts roughly to a factor of 1.2. The virtual, ideal substrate without any thermal resistance increases Q_{max} merely by a factor of 1.7. Thus plots like fig. 1-3 may help to find suitable technologies for wafer-based micro TEC fabrication. Similar plots can be calculated for different electrodes or the heat spreaders at the hot side of a peltier-cooler. Also similar qualifications plots can be calculated for thermo-generator

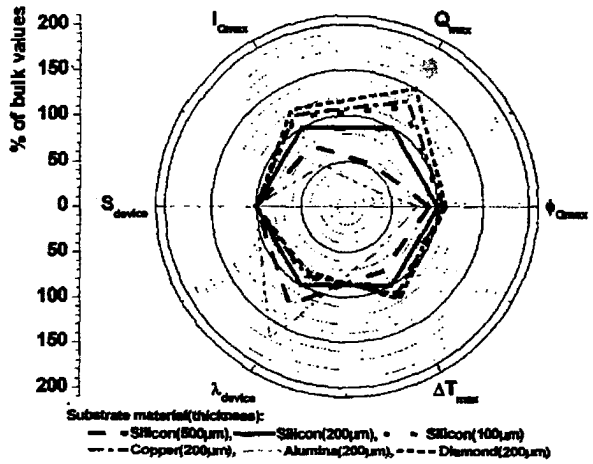

Figure 3. Performance qualification plot for different substrates. indicates Q_{max} for an "ideal" substrate without any thermal resistance

performances.

Another practical advantage is correlated to the area and shape of the performance star. If the technological results are plotted together with the simulation data accordingly, area and shape acts as a benchmark for the grade of quality of different technological and performance parameters. The more the simulation area is matched by the area derived from experimental data, the better your technology operates.

Systematics of the wafer based technologies for micro-TECs

The concepts for all the wafer technologies are quite different. Their description will be organised here as follows:

- **Devices fabricated using nanoscale technologies** comprising:
  Nanoscale CMOS devices
  Nanoscale non CMOS devices
- **Devices fabricated using MEMS technologies**

comprising:

MEMS CMOS devices

MEMS non CMOS devices

Devices fabricated using nanoscale technologies

The kick-off to explore the potential of nanoscale layered thermoelectric materials was made by Hicks, Dresselhaus and Harman [18,19,20,21]. Their approach to enhance Seebeck coeffient S (μV/K) and electrical conductivity σ $(\Omega m)^{-1}$ via two dimensional quantum well layers did not result in useable devices up to now.

Nanoscale CMOS devices

More promising, if it concerns devices in particular, are the approaches of Fan, Shakouri and LaBounty [5,6,22] who developed thermionic coolers comprising superlattices within the SiGe material system completely based on CMOS technologies [5]. They fabricated p- and n- type semidevices and demonstrated an enhancement in cooling performance compared to bulk material. At elevated temperatures of 200°C for the hot side of their thermionic cooler they measured a temperature difference across the device of 17K [5]. Due to the known decrease of the thermoelectric properties of SiGe with decreasing temperature the performance of those devices is much worse at room temperature.

Nanoscale non CMOS devices

Two different technologies have to be mentioned here: Hi-ZTechnologies [1] presented quantum well thermoelectric devices with n-type $Si/Si_{0.8}Ge_{0.2}$ and p-type B_4C and B_9C fabricated from corresponding films. But the deposition is limited to a quite small area of only $1cm^2$ [1], which is in fact not yet a common wafer technology.

The second technology is complementary to Hicks approach and linked with the name Venkatasubramanian. While Hicks et al. tried to enhance the product $S^2\sigma$ in the thermoelectric figure of merit Z [23], Venkatasubramanian intended to reduce the thermal conductivity κ (W/m*K) perpendicular to the growth plane of superlattices in the p-type Bi_2Te_3/Sb_2Te_3 and the n-type $Bi_2Te_3/Bi_2(Te,Se)_3$ material system.

The results obtained [2,24], fig.4, prove that much higher

$$Z = \frac{S^2 * \sigma}{\kappa}$$

thermoelectric efficiencies can be achieved in such superlattice structures compared to the bulk materials.

It should be mentioned that in addition to the decrease in thermal conductivity perpendicular to the superlattice plane also a decrease was found parallel to the planes [25,26] in Bi_2Te_3 based superlattices and also for the mid-temperature thermoelectric material system based on PbTe [27].

Devices fabricated using MEMS technologies

Similar to the nanoscale technologies, solely for the

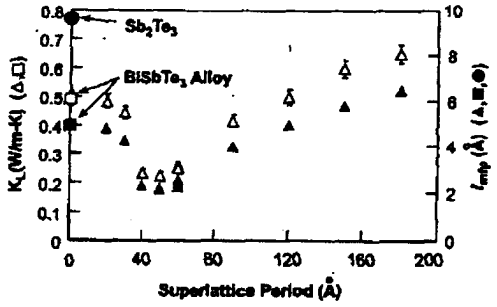

Figure 4. Decrease of lattice thermal conductivity κ_L in $(Bi,Sb)_2Te_3/Sb_2Te_3$ superlattices [24].

Bi_2Te_3 and the SiGe (for CMOS technologies) material systems micro-TECs based on wafer technologies were developed.

MEMS CMOS devices

P_3F [3] follows up the idea to combine the CMOS

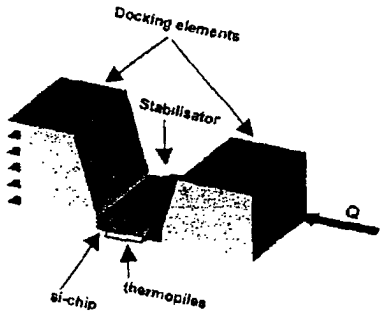

Figure 5. Scheme of the P3F TEC

microthermogenerator with typical MEMS technologies. This (P_3F) TE-device is designed in particular for harvesting waste energy.

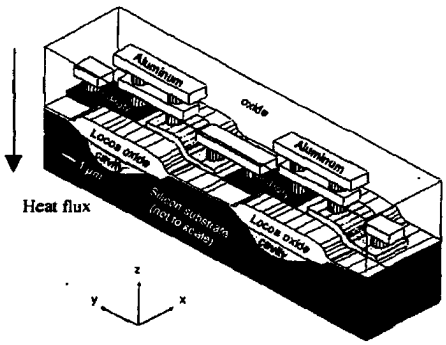

Figure 6. Schematic setup of the Infineon CMOS micro TEC [28].

The complete device consists of two docking elements for heat source and for heat spreading and in between the

micromachined TE-device. The thermocouples are made of polySi/Al. Reported performance data [3] are 19μW for ΔT=3K Figure 5 shows the schematic setup of this converter.

Also for harvesting energy Infineon [4,16,28] developed micro TE-devices using a pure 6" CMOS technology. The thermoelectric materials are n- and p-poly-Silicon or alternative poly-SiGe alloys. One specific feature is the high integration of about 60.000 thermocouples for a device of 25 mm^2. This is necessary due to the small height of about 1 μm of the thermoelectric legs brought about by the growth of so called LOCOS oxides. The resulting temperature difference across these legs amounts only to about 10 mK. The technological concept is illustrated in figure 6.

The major challenge with this approach is the dominant problem of the contact resistance. The total device resistance amounts to actually several MΩ. Aim is [4,28] to build up a generator supplying 1V under load and 1μW output power at a temperature difference of 20K placed on an area of not more than $25mm^2$.

MEMS non CMOS devices

All reported technologies were performed with Bi_2Te_3 and related compounds.

The first commercial product for microstructured Bi_2Te_3 was presented by DTS [8]. The n/p thermogenerator V-VI material is deposited with a thickness of a few μm onto Kapton® foil and structured by wet etching techniques. Details can be found in [29]. One TEC consists of ca. 2500 thermocouples and has a output power of 1 μW at ΔT=1 K.

A different method for the deposition of the thermoelectric material is chosen by Fleurial *et al.* [10,14]. The n and p thermoelectric materials are deposited electrochemically subsequently on one wafer. The patent [30] describes in detail the device technology. Advantage of this methode is the comparable easy deposition of best suitable heights of a few 10μm for the thermoelectric material, fig.1. Disadvantage is the difficulty to produce high quality material directly by electrochemical deposition. Details about the electrochemical deposition of Bi_2Te_3 and related materials may also found in [31,32]. A new approach to develop thermoelectric devices using electroplated material in a wafer technology for devices is currently started by [33,34]. In contrary to the Fleurial's concept here the n- and p-type V-VI materials are deposited and optimized on individual wafers. Advantage here is the possibility to handle independent wafers for adjusting the material quality, disadvantage is the necessity to combine the n/p-semidevices at the end of the fabrication process.

MicroTECs on Si/SiO_2 wafers made from thick sputtered V-VI compounds

Mainly aimed on telecommunication purposes, Infineon Technologies AG and Fraunhofer IPM [15] develop TECs based on the V-VI-compounds n-Bi_2Te_3 and p-$(Bi,Sb)_2Te_3$ which can be manufactured by means of regular thin film technology in combination with MEMS technologies. For the manufacturing process, the established methods in semiconductor technologies are used to deposit high quality p- and n-type materials based on V-VI compounds in thicknesses of several 10μm. We will report here on this new technology in more detail, about material and contact properties, as well as on some preliminary characteristics of first devices.

The fabrication technology is based on a two wafer process which finally leads to the devices by chip to chip, chip to wafer or wafer to wafer soldering. This "two wafers" fabrication principle requires perfectly thickness matched p- and n- material deposition, perfect over-growth of the thermoelectric material over contact electrodes and a novel dry etching techniques of the 10 μm or so thick thermoelectric material.

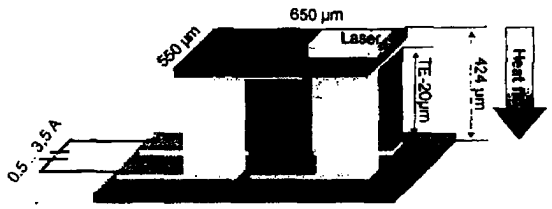

Figure 7. Schematic drawing of a possible telecommunication device

Figure 7 depicts a schematic drawing of the device application for telecommunication purposes. According to best material parameters, the following performance may be achieved for an optimum design: maximum temperature difference results to maximum net cooling of 70K; at a reduced cooling of 60K a cooling power of 0.3 W should be possible. It must be mentioned, that in this case contact resistances of $10^{-11}\Omega m^2$ were assumed.

Growth of Thermoelectric Materials

Both n-Bi_2Te_3 and p-$(Bi,Sb)_2Te_3$ materials were grown by cosputtering from 6" 99.995% element targets (Bi, Sb, Te) onto prestructured electrodes. In spite of the well known fact of the superior thermoelectric properties of the $Bi_2(Se,Te)_3$ alloys, these alloys were not grown due to delivery problems of Se-target suppliers.

The electrodes were structured on SiO_2-passivated 4"-Si-wafers. Sticking problems arise from the needed layer thickness due to huge differences of the thermal expansion coefficients for Si ($3*10^{-6}$ at 300K) [35] and e.g. Bi_2Te_3 (~14,4-21,$3*10^{-6}$ K^{-1} at 300K) [36]. Also performance problems may arise, caused by the known anisotropy of the V-VI-compounds [23,37]. A TEC, operating perpendicular to c-axis, would lead to the best device performances. Due to the chosen growth method one may expect more or less randomly aligned V-VI compound crystals.

Structural Properties

N- and p-type materials were successfully grown up to a layer thickness of about 20μm. The growth rates are in the range of 5μm/h. Thermoelectric layers were sputtered on heated (hot sputtered) as well as non-heated (cold sputtered) substrates. Substrate temperatures were taken similar to [25]. SEM analysis was used to visualise roughly the growth direction and overgrowth quality. EDX analysis was used to verify the metal/chalcogen ratio for all grown layers (accuracy ± ~0.5 at%) and to control the Bi/Sb ratio of the p-

type material, X-ray was usedfor phase analysis. After deposition an additional annealing process under controlled Te pressure is performed in order to stabilise the material properties.

A random non-textured growth can be seen, fig. 8. The left part of figure 8 shows a crack-free thermoelectric material. The cracks on its right part may be caused by the rupture of the sample during the SEM-preparation. The structural performance for hot sputtered material was proved by X-ray diffraction pattern (XRD, Θ/2Θ-analysis) [15]. EDX analysis verifiy the desired metal/ chalcogen ratio measured with an accuracy of ±~0,5at% and, in the case of p-type materials the Bi/Sb ratio with the same accuracy.

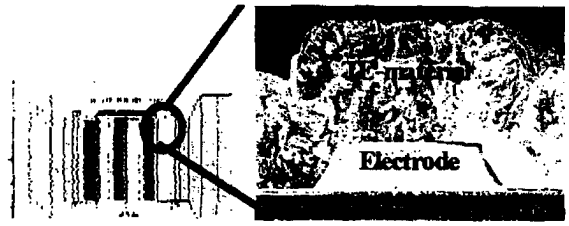

Figure 8. : SEM-picture of a cross section of a 5 µm thick p-$(Bi,Sb)_2Te_3$ layer grown over a contact electrode

For cold sputtered "BiTe" the XRD analysis shows unknown phases (certainly not Te and Bi) at about 2Θ=20° and 46° with grains in the sub-micrometer region. This is indicated by the peak broadening. After annealing the Bi/Te physical mixture aligns to textured regular Bi_2Te_3 as shown in figure 9.

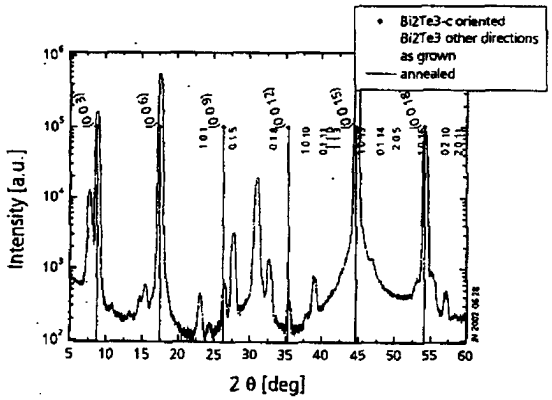

Figure 9 XRD analysis of cold sputterd Bi_2Te_3 as grown and after annealing.

Additional peaks after annealing at 2Θ=7,5°, 15° and 31°could be identified as Bi_2TeO_5 which was formed here during this annealing in a not oxygen-free atmosphere.

Thermoelectric properties

The thermoelectric properties for n- and p- type materials were determined at room temperature by van der Pauw Hall-effect and Seebeck-coefficient measurements.

The power factors were calculated using these data. The increase of the Seebeck coefficient from "cold sputtered" to "hot sputtered" is in accordance to the XRD result, fig. 9 and proves phase formation for heated substrates.

The maximum of the n/p-Seebeck coefficient appears near the existence range of the compound, fig 10a, 11a. The resulting n/p power factors are plotted in fig. 10b, 11b.

In figures 10 and 11 it is denoted with "after annealing", that a post growth annealing is performed to enhance the material performance.

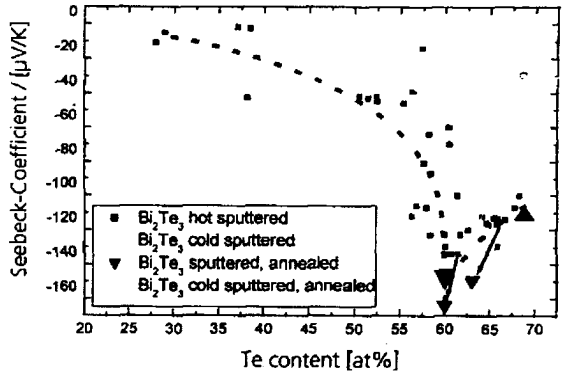

Figure 10a Seebeck coefficient vs. Te-content for the n-type-(Bi,Te) materials

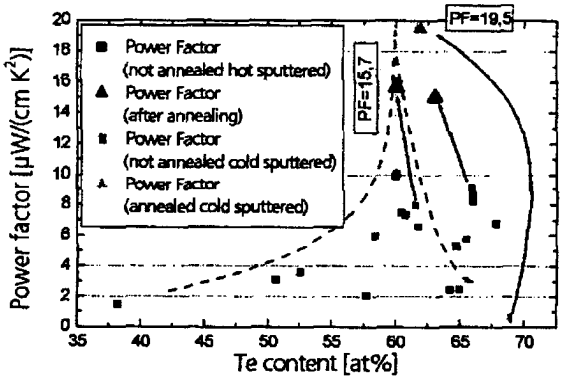

Figure 10b Power factor vs. Te-content for the n-type-(Bi,Te) materials

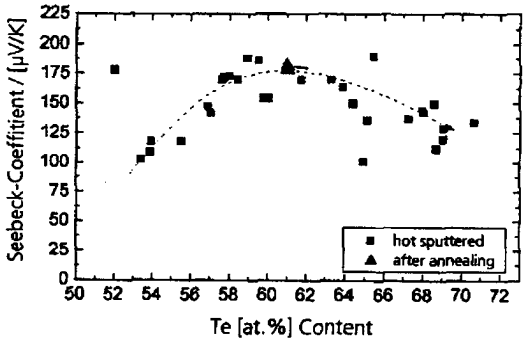

Fig.11a: Seebeck coefficient vs. Te- content for the p-type – (Bi,Sb,Te) materials

As indicated in fig 10, 11, an improvement of the Seebeck coefficient or power factor by post growth annealing is

achieved. Surprisingly the best results were achieved for annealed cold sputtered V-VI-layers.

The reason is up to now not known in detail. One may speculate about a different preferential nucleation, which favours more random alignment during simultaneous phase formation parallel to layer growth for hot sputtered compounds, and a preferential textured growth if one starts with a sub-micrometer grain mixture of the phase forming atoms or supposed pre-phases.

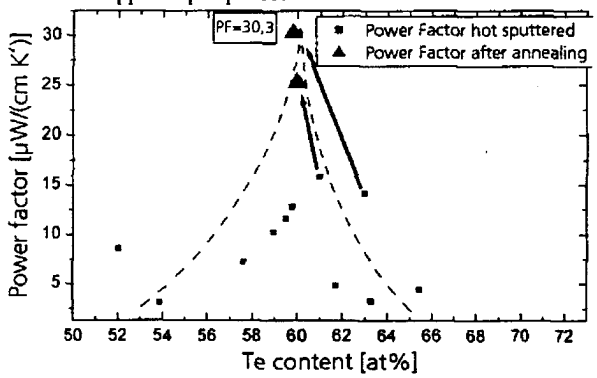

Figure 11b Power factor vs. Te-content for the n-type-(Bi,Sb,Te) materials

As the Seebeck coefficients of both annealed types are quite similar, the increase in the power factor is caused by a comparable huge increase of the electrical conductivity for the annealed cold sputtered material. The powerfactors achieved uo to now are $20\mu W/cmK^2$ and $30\mu W/cmK^2$ for n- and p-type respectively.

Device Fabrication

Before dry etching for device definition, fig. 8 left part, a solder metal is structured upon the thermoelectric material. Figure 12 shows a SEM picture of a completely etched semidevice.

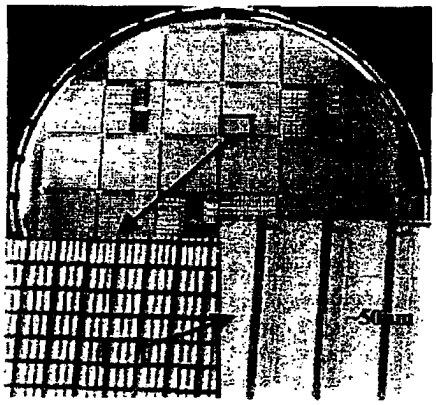

Figure 12. Processed wafer with gleamy solder, insert left down: etched semidevices for three and four thermocouples; insert right down completely etched semicouple for three thermocouples of~ 50μm width.

It can be seen, that the contact pads are insulated by small gaps in the 10 μm range. An etching angle steeper than 80° was achieved [15].

Semidevices were sawn from n- and p-wafers. The n/p-single chips are aligned to each other and then soldered together.

With devices designed for Peltier cooling, a net cooling of ΔT=10.6K was achieved. A comparison with predicted data shows, that the contact resistances are around $10^{-10}\Omega m^2$. The devices were tested for long term operation and cycling stability. A device was continuosly driven with 250 mA for one week and the net cooling was measured from time to time. The net cooling did not change, it was stable within the accuracy of the temperature measurement. Another important hint for the long term stability is the constancy after cycle tests. After 200 cycles with maximum temperature of 55°C and minimum temperature of –40°C after an overall cycle time of about 90h no significant deterioration was observed. It was also expected that the response time will decrease drastically for microTECs. Figure 13 compares the response time of this microdevice with a typical commercial cooler. The microcooler's response is about 300 times faster compared to the commercial ones.

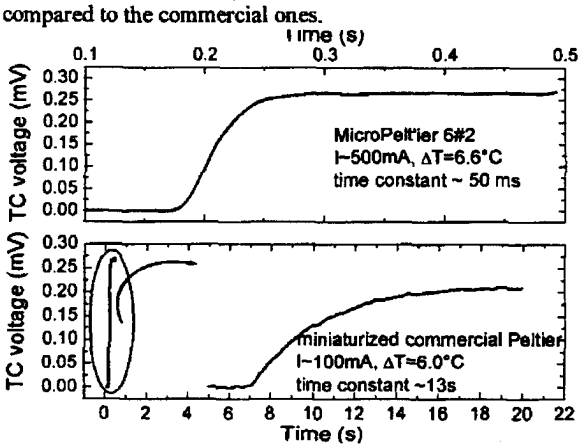

Figure 13. Comparison of the response time of this MicroTEC and the smallest commercially available device for ΔT of about 6°C.

This new technology allows the fabrication of Peltier coolers and thermogenerators. The micro-generators have the same overall dimensions as the Peltier coolers both in the range between $100\mu m^2$ to $1mm^2$. For the thermogenerators the area of the single p- and n-type elements was reduced in order to increase the number of thermocouples per unit area. In fig. 14 the electric power output of a miniaturized thermoelectric generator is plotted for different external load resistances against the temperature difference between the hot and the cold side. A maximum power output of 0.67 μW at a temperature difference of 5°C was achieved. Taking the device geometry into account this results in a power density of ~1.0 $\mu W/mm^2$.

The comparison of the results in fig.14 with the published performance data of D.T.S. [29] and Seiko [38] is shown in Table 1. The micro-thermogenerators are a factor of 10 smaller and posses only 12 thermocouples. The power output of a single thermocouple is a factor of 5 higher than reported

by Seiko and even more the 50 times larger than the values reported by D.T.S., table 1.

Since all devices use the same active thermoelectric material this result once more demonstrates the suitable material deposition, processing and packaging techniques developed for the production of miniaturized microTECs.

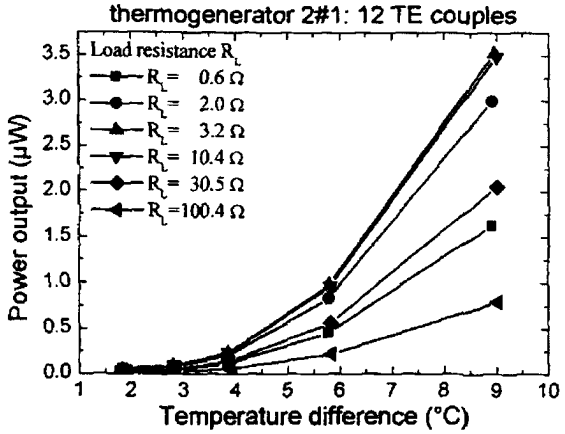

Figure 14. Dependence of the power output of a miniaturized thermoelectric generator consisting of 12 p-n-junctions for different load resistances R_L as a function of the external temperature difference.

Table 1. Comparison of miniaturized thermoelectric generators. All values are in the case of a matched load resistance and with a temperature difference of 5°K along the thermoelement.

	Area (mm^2)	Power output (µW)	Number of pn-junctions	Power / couple (nW)
D.T.S.	67.5	1.0	2500	0.4
Seiko	28.0	45.0	5000	9
MicroPelt	1.12	0.67	12	50

Conclusions

It was shown, that a fabrication of microTECs on wafer level scale is under development using different technological approaches. The materials used are preferentially based on Bi_2Te_3 related compounds or SiGe based alloys, the latter being preferred for CMOS like fabrication of microTECs. Devices with nanoscale layers or devices fabricated using bulk layers in the 10 µm range, deposited by physical vapour deposition (PVD) like sputtering [15], metal organic chemical vapour deposition (MOVCD) [2] or molecular beam epitaxy (MBE) [1] and electrochemical methods [10] and structured using MEMS technologies are under way.

If the fabrication similar to microelectronics is considered, the former disadvantage concerning the assumed impossibility to adapt microelectronic technologies for Bi_2Te_3 [5] is disproved through the new development -MicroPelt®. The successful production of these devices opens the way to new prototyping with optimised steps in the processes. Progress may be expected for the quality of the n- type material by switching to n-$Bi_2(Se,Te)_3$ [23].

A comparison of the different technological concepts is difficult due to multifaceted aspects involved. First of all the achievable material properties at the application temperature: as the most important applications for micro-devices will be around room temperature, the devices based on Bi_2Te_3 related compounds may be more favourable. For device fabrication based on wafer technologies also temperature dependent mechanical properties may play a decisive part in particular, if PVD, MOCVD or MBE deposition is necessary on heated substrates. Another major point concerns the usable technological base of well known processes, e.g. techniques to scale down lateral dimensions to get highly integrated devices. From this point of view the device fabrication based on SiGe is well stocked by existing CMOS processes. Thus up to now no clear decision can be drawn to favour only one technological route. In summary, we are convinced that micro-peltier coolers and micro-thermogenerators can be manufactured cost effectively in serial production.

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Figure 15. MicroPelt® staff

Axel Schubert as head of the Infineon part of MicroPelt®, the Fraunhofer IPM MicroPelt® team with Christa Künzel, Angela Pohlmann, Sabine Sikora-Fries, Alexander Gavrikov, Martin Jaegle, Gerd Kühner, Andreas Mahlke, Joachim Nurnus, Gerd Plescher. Also we will thank Lutz Kirste from Fraunhofer IAF for XRD-analysis. Part of the work was funded by the EC contract IST-2000-28063.

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